CLAIMS

What is claimed is:

1. A circuit, comprising:

a first depletion mode transistor having a control terminal coupled for receiving a first drive signal and a first conduction terminal coupled to a first output terminal of the circuit; and

a second depletion mode transistor having a control terminal coupled for receiving a second drive signal separate from the first drive signal, a first conduction terminal coupled to a second output terminal of the circuit, a second conduction terminal coupled to a second conduction terminal of the first depletion mode transistor.

2. The circuit of claim 1 further including:

a first current source having an output for providing a first current referenced to a voltage supply; and

a third transistor having a control terminal coupled for receiving a control signal, a first conduction terminal coupled to the first output terminal, and a second conduction terminal coupled to the output of the first current source for providing the second drive signal.

3. The circuit of claim 2 further including:

a second current source having an output for providing a second current; and

a fourth transistor having a control terminal coupled to the output of the first current source, a first conduction terminal coupled for receiving the voltage supply, and a second conduction terminal coupled to the output of the second current source for providing the first drive signal.

4. The circuit of claim 3 further including a comparator having a first input coupled for receiving the voltage supply and a second input coupled for receiving a reference voltage and an output for providing the control signal.

5. The circuit of claim 1 wherein the first depletion mode transistor is a p-channel device and the second depletion mode transistor is an n-channel device having a source coupled to the source of the p-channel device.

6. In a system, a supervisor circuit for providing a reset signal within the system in response to a voltage supply to the system, the supervisor circuit, comprising:

a detector circuit for monitoring the voltage supply and providing first and second control signals when the voltage supply falls below a predetermined value;

a first depletion mode transistor having a control terminal coupled for receiving the first control signal and a first conduction terminal coupled to a first terminal of the supervisor circuit; and

a second depletion mode transistor having a control terminal coupled for receiving the second control signal, a first conduction terminal coupled to a second terminal of the supervisor circuit, a second conduction terminal coupled to a second conduction terminal of the first depletion mode transistor.

7. The detector circuit of claim 6 further including:

a first current source having an output referenced to the voltage supply; and

a third transistor having a control terminal coupled for receiving a control signal, a first conduction terminal coupled to a first output terminal, and a second conduction terminal coupled to the output of the first current source for providing the second control signal.

8. The detector circuit of claim 6 further including:

a second current source; and

a fourth transistor having a control terminal coupled to the output of the first current source, a first conduction terminal coupled for receiving the voltage supply, and a second conduction terminal coupled to the output of the second current source for providing the first control signal.

9. The detector circuit of claim 8 further including a comparator having a first input coupled for receiving the voltage supply and a second input coupled for receiving a reference voltage and an output for providing the control signal.

10. The supervisor circuit of claim 6 wherein the first depletion mode transistor is a p-channel device and the second depletion mode transistor is an n-channel device having a source coupled to the source of the p-channel device.

11. A method of controlling first and second depletion mode transistors, comprising:

generating a first control signal;

generating a second control signal separate from the first control signal and having a state separately controlled with respect to the first control signal;

controlling the first and second depletion mode transistors connected in a series arrangement in response to the first and second control signals.

12. The method of claim 11, wherein the step of controlling the first and second depletion mode transistors includes enabling the first and second depletion mode transistors when the first and second control signals have first complementary states.

13. The method of claim 11, wherein the step of controlling the first and second depletion mode transistors includes disabling the first and second depletion mode transistors when the first and second control signals have second complementary states.

14. The method of claim 11, further including providing a reset signal when the first and second depletion mode transistors are enabled by the first and second control signals having first complementary states.

15. A circuit, comprising:

first and second depletion mode transistors coupled in series between first and second terminals of the circuit and operating in response to first and second separate control signals.

16. The circuit of claim 15 further including:

a first current source; and

a third transistor having a control terminal coupled for receiving a control signal, a first conduction terminal coupled to the first terminal of the circuit, and a second conduction terminal coupled to the output of the first current source for providing the second control signal.

17. The circuit of claim 15 further including:

a second current source; and

a fourth transistor having a control terminal coupled to the output of the first current source, a first conduction terminal coupled to a third terminal of the circuit, and a second conduction terminal coupled to the output of the second current source for providing the first control signal.

18. The supervisor circuit of claim 15 wherein the first depletion mode transistor is a p-channel device and the second depletion mode transistor is an n-channel device having a common source with the p-channel device.

19. A method of controlling first and second series connected depletion mode transistors comprising the step of generating first and second separate control signals to operate the first and second series connected depletion mode transistors.

20. The method of claim 19, wherein the step of generating includes receiving a first compared signal and enabling the first control signal and disabling the second control signal in response to the first compared signal.

21. The method of claim 19, wherein the step of generating includes receiving a second compared signal and disabling the first control signal and enabling the second control signal in response to the second compared signal.

22. The method of claim 19, wherein the step of operating includes operating the first and second series connected depletion mode transistors in response to a voltage supply having a value down to zero volts.

23. A linear regulator circuit having an input coupled for receiving an input voltage and providing at an output terminal a regulated output voltage, comprising:

a first depletion mode transistor having a control terminal coupled for receiving a first drive signal and a first conduction terminal coupled to the input of the linear regulator circuit;

a second depletion mode transistor having a control terminal coupled for receiving a second drive signal separate from the first drive signal, a first conduction terminal coupled to the output terminal of the linear regulator circuit, and a second conduction terminal coupled to a second conduction terminal of the first depletion mode transistor; and

a control circuit having first and second outputs for providing the first and second drive signals respectively which control the first and second depletion mode transistors to provide the regulated output voltage.

24. The regulator circuit of claim 23 further including a controller having first and second independently controlled outputs for coupling to the control terminals of the first and second depletion mode transistors.

25. The regulator circuit of claim 23 wherein the first depletion mode transistor is an n-channel device and the second depletion mode transistor is a p-channel device

having a source coupled to the source of the n-channel device.

26. The regulator circuit of claim 23 wherein the first depletion mode transistor is a p-channel device and the second depletion mode transistor is an n-channel device having a source coupled to the source of the p-channel device.